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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/676,137	09/30/2003	Frank E. LeClerg	884.A46US1	6409

21186 7590 10/30/2007

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EXAMINER	
KERVEROS, JAMES C	

ART UNIT	PAPER NUMBER
2117	

MAIL DATE	DELIVERY MODE
10/30/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/676,137	LECLERG ET AL.	
	Examiner	Art Unit	
	JAMES C. KERVEROS	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 October 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09/30/2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This is a Final Office Action in response to the AMENDMENT filed 10/15/2007.

Claims 1-25 are presently under examination and pending.

Response to Arguments

Applicant's arguments filed on 10/15/2007, with respect to the rejection of claims 1-25 under 35 U.S.C. 102(e) as being anticipated by Moyes et al. (US 7,065,688), have been fully considered but they are not persuasive.

In response to Applicant's argument that Moyes is not prior art to the present application, the Examiner notes that the US Application for the Moyes US Patent 7,065,688 was filed on 2/19/2003, which predates the filing date 09/30/2003 of the present application. Therefore, based upon the earlier effective U.S. filing date of the Moyes reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Applicant argues, with respect to the rejection of claims 1-25 under 35 U.S.C. § 102(e), that Moyes describes a memory initialization and testing at the "processor level", while in contrast, the subject matter of the present application performs memory initialization and testing at the "memory module level", which is finer grain and allows parallel initialization and testing at a greater level.

In response to Applicant's argument, the Examiner notes that the limitation, memory initialization and testing at the "processor level" in comparison with the memory initialization and testing at the "memory module level" is not part of the claims and, further, the "processor level" in comparison with the "memory module level" is relative terminology, which is indefinite under 35 U.S.C. 112, second paragraph, since the term is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

In response to applicant's argument, with respect to the features upon which applicant relies in his arguments (i. e., initialization and testing at the "processor level" versus at the "memory module level") are not recited in the rejected claims. Although the claims are interpreted in light of the specification, limitations from the specification or Applicant's arguments are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Furthermore, the "memory module level" initialization and testing is a subjective definition by the Applicant and does not necessarily imply a lower level testing in comparison to a higher "processor level" by Moyes as alleged by the Applicant.

According to the Summary of the Invention present invention, Moyes describes that each processor initializes a portion of memory significantly improving memory initialization time by allowing initialization to occur concurrently for multiple memory locations and by eliminating communication time for the BSP to access distant memory.

Each processing node in the multi-processor system tests and initializes its "own local memory". Each processing node 202 is associated with the initialization and testing of a corresponding memory array 206, Fig. 2, where each memory array 206 consists of several (dual inline memory modules) DIMM, which make up a memory array 206, and where a DIMM contains multiple random access memory (RAMs) 402, as shown in Fig. 4, and where (RAMs) 402 correspond to Applicant's memory modules 112, 114, 116 in Fig. 1.

Clearly, Moyes discloses initialization and testing of random access memory (RAMs) 402 at the module level associated with memory array 206.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Moyes et al. (US 7,065,688) filed: 2/19/2003.

Regarding independent Claims 1, 5, 8, 12, 16, 21, Moyes discloses a method for simultaneous multiprocessor memory testing and initialization during system boot, as illustrated by the flow diagram of Fig. 5, for optimized memory testing and initialization, comprising:

Performing a memory access procedure (step 502) by initializing system links such that each processing node can communicate to other processing nodes and memory, performed by BIOS running on the bootstrap processor (BSP), which causes the memory initialization process to begin (step 504). The BSP can send a start message to each processing node or a broadcast message to all processing nodes. Alternatively, a bit can be written in each processing node indicating the memory initialization and testing process is to begin.

Each processing node performs memory initialization and testing for a portion of memory, step 506, as also illustrated in Fig. 2, thus, having each processing node initialize and test its own local memory, by executing a routine that tests and initializes memory.

Regarding Claims 2-4, 6, 7, 9-11, 13-15, 17-20, 22-25, Moyes discloses each processing node reports status, step 508, which occurs, for example, continuously during the memory initialization and test, periodically, or when memory initialization and testing are complete. After all processing nodes have completed memory initialization and test, the bootstrap processor continues with system boot and the other processing nodes halt, step 510.

Fig. 6 illustrates an exemplary status reporting mechanism 600, using periodic status reporting from the various processing nodes, where the boot strap processor can create a display for a computer screen depicting the current status, displays 602 [0:N] depicting a percent completion of the memory initialization and testing process on each processing node and/or overall.

Regarding Claims 7, 8, 10, Moyes discloses error correction code (ECC) chip 404, which stores error correction codes that allow memory errors to be found and corrected. Additionally, DIMM 400 can have an SPD (serial presence detect) chip 406, which contains read only information specifying an operational range of DIMM 400 and other information similar to what one would find in a data sheet. For example, SPD chip 406 identifies memory storage capacity of DIMM 400, operating parameters such as minimum cycle times, CAS latency, Fig. 4.

Upon system initialization, each memory module must be initialized and tested. This can include verifying population of memory modules, verifying proper operation of the memory (no stuck bits), and initializing or clearing the memory to known values. Each memory module can be scrubbed on a periodic basis utilizing ECC to correct any memory errors.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques H. Louis-Jacques can be reached on (571) 272-4150. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Date: 24 October 2007
Office Action: Final Rejection

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